ABHINANDAN MAJUMDAR

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EDUCATION

Cornell University, Ithaca NY **Aug 2011 – Aug 2017**
Doctor of Philosophy, Electrical and Computer Engineering **GPA: 3.9/4.0**
Thesis: *Proactive Energy Management Techniques for Smart Building and Server Architectures*
Committee: Prof. David H. Albonesi (Advisor), Prof. Brandon Hencey, Dr. Indrani Paul, Prof. Bart Selman, Prof. Zhiru Zhang

Cornell University, Ithaca NY **Aug 2011 – Jan 2016**
Master of Science, Electrical and Computer Engineering

Columbia University, New York NY **Aug 2007 – Dec 2008**
Master of Science, Computer Engineering **GPA: 3.9/4.0**

National Institute of Technology Karnataka, Surathkal, India **June 2006**
Bachelor of Engineering, Computer Science and Engineering **Aggregate: 81%**

PROFESSIONAL EXPERIENCE

Intel Corporation **Sep 2017 - Present**
Power Management Architect, Platform Architecture Group
- Defining the power management architecture of upcoming Intel processors.

AMD Research, Advanced Micro Devices Inc., Austin TX **Jan 2015 – Sep 2015, Jan 2016 – Jun 2016**
Co-op Engineer, Heterogeneous Processor Power Management, Dr. Indrani Paul
- Developing proactive methods to reduce processor-level energy consumption without impacting application performance.

Computer Systems Laboratory, Cornell University, Ithaca NY **Aug 2011 – Aug 2017**
Graduate Research Assistant, Smart Buildings, Prof. David H. Albonesi
- Developing proactive methods to reduce HVAC energy cost of a building by learning and shaping the occupancy profiles.

NEC Research Laboratories, Princeton NJ **Feb 2009 – June 2011**
Research Assistant, Universal Learning Machine, Dr. Srihari Cadambi
- Designed and implemented MAPLE processor on Xilinx Virtex 5 FPGA to accelerate machine learning applications.

Intel Technology, Bangalore, India **July 2006 – July 2007**
Software Engineer, Intel® Turbo Memory Module, Mr. Sriram Ranganathan
- Provided driver support, and developed ReadyBoost and ReadyDrive features for Intel Turbo Memory.

Indian Institute of Technology, Delhi, India **June 2005 – July 2005**
Summer Intern, FPGA Implementation of Integer Linear Programming Accelerator, Prof. M. Balakrishnan
- Designed and implemented simplex algorithm on Xilinx Virtex II FPGA, and obtained a speed-up over the C implementation.

SELECTED PUBLICATIONS

- **Abhinandan Majumdar**, Leonardo Piga, Indrani Paul, Joseph L. Greathouse, Wei Huang and David H. Albonesi, "Dynamic GPGPU Power Management using Adaptive Model Predictive Control," *23rd IEEE Symposium on High Performance Computer Architecture*, Austin, February 2017.
- **Abhinandan Majumdar**, Zhiru Zhang, and David H. Albonesi, "Characterizing the Benefits and Limitations of Smart Building Meeting Room Scheduling," *International Conference on Cyber Physical Systems*, Vienna, April 2016.
- **Abhinandan Majumdar**, Gene Wu, Kapil Dev, Joseph L. Greathouse, Indrani Paul, Wei Huang, Arjun-Karthik Venugopal, Leonardo Piga, Chip Freitag, and Sooraj Puthoor, "A Taxonomy of GPGPU Performance Scaling," *IEEE International Symposium on Workload Characterization*, Atlanta, October 2015.
- **Abhinandan Majumdar**, Jason L. Setter, Justin R. Dobbs, Brandon M. Hencey, and David H. Albonesi, "Energy-Comfort Optimization using Discomfort History and Probabilistic Occupancy Prediction," *International Green Computing Conference*, Dallas, November 2014.
- **Abhinandan Majumdar**, David H. Albonesi, and Pradip Bose, "Energy-Aware Meeting Scheduling Algorithms for Smart Buildings," *4th ACM Workshop On Embedded Sensing Systems For Energy-Efficiency In Buildings*, November 2012.
- **Abhinandan Majumdar**, Srihari Cadambi, Michela Becchi, Srimat T. Chakradhar, and Hans Peter Graf, "A Massively Parallel, Energy Efficient Programmable Accelerator for Learning and Classification," *ACM Transactions of Architecture and Code Optimization*, Vol. 9, No. 1, Article 6, March 2012.
- Srihari Cadambi, **Abhinandan Majumdar**, Michela Becchi, Srimat T. Chakradhar, and Hans Peter Graf, "A Programmable Parallel Accelerator for Learning and Classification," *19th International Conference on Parallel Architectures and Compilation Techniques*, September 2010.

PATENTS

- **Abhinandan Majumdar**, Brian Kocoloski, Leonardo Piga, Wei Huang, and Yasuko Eckert, "Temperature-Aware Task Scheduling and Proactive Power Management", US Patent App. No. 15/192784, filed June 2016.
- Leonardo Piga, Brian Kocoloski, Wei Huang, **Abhinandan Majumdar**, and Indrani Paul, "Real-Time Performance Tracking Using Dynamic Compilation", US Patent App. No. 15/192748, filed June 2016.
- Wei Huang, Manish Arora, **Abhinandan Majumdar**, Indrani Paul, and Leonardo Piga "Method and Apparatus for Managing Power in a Thermal Couple Aware System," US Patent Application No. 15/071,643, filed Mar 2016.
- Leonardo Piga, **Abhinandan Majumdar**, Indrani Paul, Wei Huang, Manish Arora, and Joseph L. Greathouse, "Hardware Accuracy Counters for Application Precision and Quality Feedback," US Patent Application No. 14/981,310, filed Dec 2015.
- **Abhinandan Majumdar**, Srihari Cadambi, and Srimat T. Chakradhar, "Energy-efficient Heterogeneous Systems," US Patent 8,874,943 B2, issued Oct 2014.
- Srihari Cadambi, **Abhinandan Majumdar**, Michela Becchi, Srimat T. Chakradhar, and Hans Peter Graf, "Massively Parallel, Smart Memory-based Accelerator," US Patent 8,583,896 B2, issued Nov 2013.

COURSE/RESEARCH PROJECTS

EmoDetect – Smart Emotion Detection from Facial Expressions **Fall 2012**

- Developed a classifier to recognize the emotions from images using machine learning and feature extractor algorithms.

I/O Placement and Floorplanning of 16 core Network On Chip **Jan 2008 – Feb 2009**

- Implemented the physical design of NoC and performed the I/O placement using IBM 90nm technology.

Design of a MOS-based Transimpedance Amplifier for a Transceiver-level Receiver Application **Fall 2008**

- Designed a two stage amplifier to achieve a transimpedance gain of 3.49kΩ and a bandwidth of 2.96GHz.

Vulnerability of On-chip Interconnection Networks to Soft Errors **Spring 2008**

- Designed an RTL architecture of wormhole router, and projected a linear increase in the soft error with technology scaling.

FPGA Implementation of AES Decryptor **Spring 2008**

- Designed and implemented the AES decryption algorithm on Altera Cyclone II FPGA.

4 Kilobyte SRAM Array using IBM 90nm Technology **Fall 2007**

- Designed and implemented a DRC/LVS clean design of address decoder and 64x64 SRAM array.

RELEVANT COURSE WORK

Graduate	Computer Architecture, Parallel Computer Architecture, Memory Systems, Digital VLSI, Embedded System Design, Analog Circuits, Digital Signal Processing, Artificial Intelligence, Machine Learning, Feedback Control Systems, Stochastic Optimal Control.
Undergraduate	Digital Design, Microprocessors, Computer Organization, Operating Systems, Algorithms, Database, Compilers, Digital Communication, Computer Networks, Data Structures, Programming Languages.

TEACHING EXPERIENCE

TA, Digital Logic and Computer Organization, Cornell University	Fall 2016
TA, Modern Computing Devices, Cornell University	Fall 2012, Summer 2016
TA, Introduction to Circuits, Cornell University	Fall 2015
TA, Advanced Logic Design, Columbia University	Spring/Fall 2008
TA, Fundamentals of Computer Systems, Columbia University	Fall 2007, Spring/Fall 2008

TECHNICAL SKILLS

Hardware	Virtuoso, HSPICE, Spectre, Ultrasim, Encounter, Calibre DRC/LVS/xRC, VHDL, Verilog, Quartus, ISE, ModelSim.
Software	C/C++, CUDA, Java, Matlab, Perl, Python, SQL, CVX, CPLEX, clasp, lpsolve, EnergyPlus.

PROFESSIONAL SERVICE

- *Submissions Co-chair* for ISCA'15.
- *Reviewer* for ASPLOS 2017, JAISE 2017, ACM TACO and IEEE Robotics and Automation.
- *President* of Cornell India Association 2013 – 2014.

AWARDS

- *Outstanding Teaching Assistant 2017,* Electrical and Computer Engineering Department, Cornell University.
- *Jacobs Scholar Fellowship*, Cornell University.
- *MS Teaching Assistant Fellowship* from Computer Science Department, Columbia University.