

ABHINANDAN MAJUMDAR

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RESEARCH Energy-efficient Computer Architecture, High Performance Computing, Machine
INTERESTS Learning, and Artificial Intelligence, and Building Automation and Controls.

EDUCATION Ph.D., Electrical and Computer Engineering 2011 – Aug 2017
Thesis: “*Proactive Energy Management Techniques for Smart Building and Server Architectures*”
Advisor: *Prof. David H. Albonesi* GPA: 3.9/4.0
Committee: *Prof. Brandon M. Hency, Prof. Bart Selman, Prof. Zhiru Zhang, and Dr. Indrani Paul*
Cornell University, Ithaca, NY

M.S., Computer Engineering 2007 – 2008
Columbia University, New York, NY GPA: 3.9/4.0

B.E., Computer Engineering 2002 – 2006
National Institute of Technology Karnataka, Surathkal, India Aggregate: 81%

PROFESSIONAL Power Management Architect, Platform Architecture Group Sep 2017– Present
EXPERIENCE Intel Corporation, Hillsboro, OR

Co-op Engineer, AMD Research Jan 2016 – June 2016
Advanced Micro Devices, Inc., Austin, TX Jan 2015 – Sep 2015

Research Assistant, System Architecture Department Feb 2009 – June 2011
NEC Laboratories America, Inc., Princeton, NJ

Software Engineer, Mobility Group of India July 2006 – July 2007
Intel Corporation, Bangalore, India

Summer Intern, Computer Science and Engineering June 2005 – July 2005
Indian Institute of Technology Delhi, India

REFEREED Abhinandan Majumdar, Leonardo Piga, Indrani Paul, Joseph L. Greathouse, Wei Huang
PUBLICATIONS and David H. Albonesi, “Dynamic GPGPU Power Management using Adaptive Model Predictive Control,” 23rd IEEE Symposium on High Performance Computer Architecture, Austin, February 2017 [Acceptance Rate: 22%].

Abhinandan Majumdar, Zhiru Zhang, and David H. Albonesi, “Characterizing the Benefits and Limitations of Smart Building Meeting Room Scheduling,” *7th International Conference on Cyber-Physical Systems*, April 2016 [Acceptance Rate: 28%].

- REFEREED PUBLICATIONS
- Abhinandan Majumdar, Gene Wu, Kapil Dev, Joseph L. Greathouse, Indrani Paul, Wei Huang, Arjun-Karthik Venugopal, Leonardo Piga, Chip Freitag, and Sooraj Puthoor, “A Taxonomy of GPGPU Performance Scaling,” *IEEE International Symposium on Workload Characterization*, October 2015 [Acceptance Rate: 48%].
- Abhinandan Majumdar, Jason L. Setter, Justin R. Dobbs, Brandon M. Hency, and David H. Albonesi, “Energy-Comfort Optimization using Discomfort History and Probabilistic Occupancy Prediction,” *International Green Computing Conference*, November 2014 [Acceptance Rate: 36%].
- Abhinandan Majumdar, David H. Albonesi, and Pradip Bose, “Energy-Aware Meeting Scheduling Algorithms for Smart Buildings,” *4th ACM Workshop On Embedded Sensing Systems For Energy-Efficiency In Buildings*, November 2012 [Acceptance Rate: 32%].
- Abhinandan Majumdar, Srihari Cadambi, Srimat T. Chakradhar, and Hans Peter Graf, “An FPGA-based Parallel Accelerator for Semantic Search,” *9th IEEE Symposium on Application Specific Processors*, June 2011 [Acceptance Rate: 29%].
- Srihari Cadambi, Abhinandan Majumdar, Michela Becchi, Srimat T. Chakradhar, and Hans Peter Graf, “A Programmable Parallel Accelerator for Learning and Classification,” *19th International Conference on Parallel Architectures and Compilation Techniques*, September 2010 [Acceptance Rate: 17%].
- JOURNALS
- Abhinandan Majumdar, Srihari Cadambi, Michela Becchi, Srimat T. Chakradhar, and Hans Peter Graf, “A Massively Parallel, Energy Efficient Programmable Accelerator for Learning and Classification,” *ACM Transactions of Architecture and Code Optimization*, Vol. 9, No. 1, Article 6, March 2012.
- Abhinandan Majumdar, Srihari Cadambi, and Srimat T. Chakradhar, “An Energy-Efficient Heterogeneous System for Embedded Learning and Classification,” *IEEE Embedded Systems Letters*, Vol. 3, No. 1, March 2011.
- BOOK CHAPTERS
- Igor Durdanovic, Eric Cosatto, Hans Peter Graf, Srihari Cadambi, Venkat Jakkula, Srimat T. Chakradhar, and Abhinandan Majumdar, “Massive SVM Parallelization using Hardware Accelerators,” *Scaling Up Machine Learning*, Cambridge University Press, 2011.
- POSTERS
- Abhinandan Majumdar, David H. Albonesi, Howard Chong, Brandon M. Hency and Christine A. Shoemaker, “Adaptive Comfort Control and Automated Meeting Assignment for Smart Buildings,” *Atkinson Center for a Sustainable Future*, Cornell University, Ithaca, NY, October 2014.
- Rishabh Animesh, Skand Hurkat, Abhinandan Majumdar, and Aayush Saxena, “EmoDetect – Smart Emotion Detection from Facial Expressions,” *BOOM*, Cornell University, Ithaca, NY, April 2013.

POSTERS Srihari Cadambi, Bing Bai, Iain Melvin, Abhinandan Majumdar, Igor Durdanovic, Hans Peter Graf, and Srimat T. Chakradhar, “Massively Parallel Low-Power Processor for Learning and Classification,” *Neural Information Processing Systems*, Vancouver, BC, December 2009.

PATENTS Abhinandan Majumdar, Brian Kocoloski, Leonardo Piga, Wei Huang, Yasuko Eckert, “Temperature-Aware Task Scheduling and Proactive Power Management,” US Patent Application No. 15/192,784, filed June 2016.

Leonardo Piga, Brian Kocoloski, Wei Huang, Abhinandan Majumdar, Indrani Paul, “Real-Time Performance Tracking Using Dynamic Compilation,” US Patent Application No. 15/192,748, filed June 2016.

Wei Huang, Manish Arora, Abhinandan Majumdar, Indrani Paul, and Leonardo Piga “Method and Apparatus for Managing Power in a Thermal Couple Aware System,” US Patent Application No. 15/071,643, filed March 2016.

Leonardo Piga, Abhinandan Majumdar, Indrani Paul, Wei Huang, Manish Arora, and Joseph. L. Greathouse, “Hardware Accuracy Counters for Application Precision and Quality Feedback,” US Patent Application No. 14/981,310, filed December 2015.

Abhinandan Majumdar, Srihari Cadambi, and Srimat T. Chakradhar, “Energy-efficient Heterogeneous Systems,” US Patent 8,874,943 B2, issued October 2014.

Srihari Cadambi, Abhinandan Majumdar, Michela Becchi, Srimat T. Chakradhar and Hans Peter Graf, “Massively Parallel, Smart Memory-based Accelerator,” US Patent 8,583,896 B2, issued November 2013.

RESEARCH Graduate Research Assistant, Cornell University, Ithaca, NY 2011 – Aug 2017

EXPERIENCE Advisor: *Prof. David H. Albonese*

Collaborators: *Prof. Brandon M. Hincey* and *Prof. Zhiru Zhang*

- Developing smart building HVAC control algorithms based on dynamic characterization and prediction of occupant activities, building model, and weather factors.
 - Developed energy-efficient meeting assignment algorithms for smart buildings
 - Proposed a meeting room energy model by characterizing the building power.
 - Developed search algorithms, and 0-1 ILP model to determine best meeting assignment.
 - Demonstrated significant energy savings and better scalability for larger problem sets.
 - Identified situations where smart meeting assignment algorithms are promising, and when is it not worthwhile.

RESEARCH
EXPERIENCE

- Extended the energy model to include weather and solar effects.
- Published at ICCPS'16 and BuildSys'12.
- Balancing Energy and Comfort via Probabilistic Occupancy Prediction Control
 - Using Model Predictive Control, dynamically balanced HVAC energy and occupant discomfort by learning the occupancy pattern.
 - Demonstrated significant energy savings while operating within an allowed discomfort limit.
 - Published at IGCC'14.

Co-op Engineer, AMD Research, Austin, TX

Jan 2016 – Jun 2016

Collaborators: *Dr. Indrani Paul, Dr. Leonardo Piga, Dr. Joseph L. Greathouse, Dr. Wei Huang, and Prof. David H. Albonesi*

Jan 2015 – Sep 2015

- Developed proactive techniques to improve GPGPU energy efficiency without impacting performance.
 - Proposed Model Predictive Control to reduce GPGPU energy while tracking a performance target.
 - Developed a GPGPU power and performance prediction model using machine learning algorithms.
 - Demonstrated significant energy savings with negligible performance impact.

Research Assistant, NEC Laboratories America, Princeton, NJ

2009 – 2011

Supervisor: *Dr. Srihari Cadambi*

- Designed MAPLE - an FPGA-based massively parallel, energy efficient, smart memory-based accelerator for learning and classification applications.
- Published at PACT'10, SASP'11, ACM TACO'12.

Tape-out of 16 Core Network On Chip to test the feasibility of 4GHz on-chip communication

2008 – 2009

Advisor: *Prof. Kenneth Shepard, Columbia University*

- Implemented the physical design of the NoC and performed I/O placement of the NoC using IBM 90nm CMOS technology.

Vulnerability of On-Chip Networks to Soft Errors

Spring 2008

Advisor: *Prof. Simha Sethumadhavan, Columbia University*

- Analyzed Soft Error Rate for on-chip routers designed using 90nm to 22nm CMOS technology, and projected down to 11nm technology.

RESEARCH EXPERIENCE	<p>Software Engineer, Intel Technologies, Bangalore, India Supervisor: <i>Mr. Sriram Ranganathan</i></p> <ul style="list-style-type: none"> • Performed driver development for ReadyBoost and ReadyDrive technologies and verification support for Intel Turbo Memory. • Developed a user-managed drag-and-drop tool to cache frequently used applications and data on Intel Turbo Memory. <p>Summer Intern, Indian Institute of Technology, Delhi Advisor: <i>Prof. M. Balakrishnan</i></p> <ul style="list-style-type: none"> • Implemented FPGA Accelerator for Integer Linear Programming Algorithm. 	<p>2006 – 2007</p> <p>June – July 2005</p>
ACADEMIC PROJECTS	<p>EmoDetect – Smart Emotion Detection from Facial Expressions Course: <i>Machine Learning</i> Instructor: <i>Prof. Thorsten Joachims, Cornell University</i></p> <ul style="list-style-type: none"> • Developed an emotion detection scheme using a combination of different extraction and machine learning algorithms. • Extraction algorithms involved Gabor, Histogram of Gradients, Haar and Moments • Machine learning algorithms involved SVM, Random Trees and ANN. • Gabor+SVM showed an accuracy of 63% on untrained facial samples. • Awarded the Best Machine Learning course project among ~30+ project teams, each comprising of 3-4 students. • Awarded the Yahoo Student Research Award and Morgan Stanley Innovation Award at Boom 2013. <p>Heuristic Optimization Algorithms for Energy Efficient Meeting Scheduling Course: <i>Heuristic Methods for Optimization</i> Instructor: <i>Prof. Christine Shoemaker, Cornell University</i></p> <ul style="list-style-type: none"> • Studied performance of heuristic optimization algorithms (Random Sampling, Greedy Stochastic, Simulated Annealing, Genetic Algorithm and Tabu Search). • Proposed two algorithmic variations – constrained neighborhood search and selective perturbation. • Observed Greedy Stochastic to be the best optimization algorithm, and Tabu Search the worst. 	<p>Fall 2012</p> <p>Fall 2012</p>

ACADEMIC PROJECTS	<p>FPGA-based 128 bit AES Decryptor Course: <i>Embedded Systems Design</i> Instructor: <i>Prof. Stephen Edwards, Columbia University</i></p> <ul style="list-style-type: none"> Designed an FPGA-based system that reads a sequence of encrypted images from a high-latency SD-CARD, decrypts it in on-the-fly, and displays it at a real-time on a VGA (as an animation) with a high frame rate. 	Spring 2008
	<p>HW/SW Optimization of Matrix Multiplication Course: <i>Computer Architecture</i> Instructor: <i>Prof. Luca Carloni, Columbia University</i></p> <ul style="list-style-type: none"> Reduced the run-time of a series of matrix-multiplications by optimizing the software implementation and architectural configuration using SESC simulator. 	Fall 2007
	<p>64x64 bit SRAM design Course: <i>Digital VLSI Circuits</i> Instructor: <i>Prof. Azeez Bhavnagarwala, Columbia University</i></p> <ul style="list-style-type: none"> Performed a full custom physical design of SRAM array along with address decoder, precharge circuit, read-sense amplifier and write driver using IBM 90nm CMOS technology. 	Fall 2007
	<p>MOS-based Transimpedance Amplifier Course: <i>Analog Systems Design</i> Instructor: <i>Prof. Timothy Dickson, Columbia University</i></p> <ul style="list-style-type: none"> Designed a transimpedance amplifier with a gain of 3k-ohms, a bandwidth of 2.8 GHz, and a group-delay variation of 40ps. 	Fall 2008
TEACHING EXPERIENCE	<p>TA, Digit Logic and Computer Organization, Cornell University TA, Modern Computing Devices (Online), Cornell University TA, Introduction to Circuits, Cornell University TA, Modern Computing Devices, Cornell University TA, Advanced Logic Design, Columbia University TA, Fundamentals of Computer Systems, Columbia University</p>	<p>Fall 2016 Summer 2016 Fall 2015 Fall 2012 Spring/Fall 2008 Spring/Fall 2008</p>
AWARDS	<p><i>Outstanding Teaching Assistant Award 2017</i>, Electrical and Computer Engineering Department, Cornell University.</p> <p><i>Yahoo Student Research Award</i> and <i>Morgan Stanley Innovation Award</i> at Boom 2013, Cornell University.</p> <p>Best in-class Machine Learning course project, Cornell University.</p> <p><i>Jacobs Scholar Fellowship</i>, Cornell University.</p> <p><i>MS Teaching Assistant Fellowship</i>, Columbia University.</p> <p><i>Spontaneous Recognition Award</i>, Intel Technology, Bangalore.</p>	

AWARDS	<p><i>Best Student Paper Award</i> at International Conference on Systemics, Cybernetics and Informatics 2006.</p> <p><i>Best Student Of The Year Award</i> for obtaining 1st position (90.4%) out of ~150 students in CBSE 12th board exam by DAV Public School, Bilaspur, India.</p> <p><i>2nd position</i> (out of ~10,000 applicants) in Chhattisgarh Pre-Engineering Test 2002.</p> <p><i>All India Rank 244</i> and <i>State Rank 6th</i> (out of ~one million applicants) in All India Engineering Entrance Examination 2002.</p>	
SKILLS	<p><i>Simulators:</i> EnergyPlus, SESC, SimpleScalar</p> <p><i>Optimization tools:</i> CVX, CPLEX, clasp, lpsolve</p> <p><i>Languages:</i> C, CUDA, Java, Matlab, Perl, Python, SQL</p> <p><i>VHSIC:</i> VHDL, Verilog</p> <p><i>FPGA tools:</i> Xilinx ISE, Altera's Quartus</p> <p><i>CAD tools:</i> Google Sketchup, OpenStudio, Virtuoso Schematic/Layout, SoC Encounter, HSPICE, Spectre, UltraSim, Calibre DRC/LVS/xRC, ModelSim</p>	
RELEVANT COURSES	<p><i>Doctoral (Cornell):</i> Parallel Computer Architecture, Memory Systems, Machine Learning, Artificial Intelligence, Digital Feedback Control, Feedback Control Systems, Multivariable Feedback Control, Stochastic Optimal Control, Process Control Strategies, Heuristic Methods for Optimization.</p> <p><i>Online:</i> Convex Optimization, Linear Optimization</p> <p><i>Masters (Columbia):</i> Computer Architecture, Embedded System Design, Distributed Embedded System, VLSI Circuits, Analog Electronic Circuits, Topics in Electronic Circuits, Digital Signal Processing, Formal Verification</p> <p><i>Undergraduation (NITK):</i> Digital Systems, Logic Design, Computer Organization, Computer Architecture, Microprocessors, Operating Systems, Algorithms, Computer Networks, Graphics, Database Systems, Compilers, Data Structures, Programming Languages, Software Engineering, Operations Research, Object Oriented Systems, Data Communications, Theory of Computation, Systems Programming, Principles of Programming Languages.</p>	
PROFESSIONAL SERVICE	<p>Shadow PC Reviewer, ASPLOS</p> <p>Reviewer, IEEE Robotics and Automation Letters</p> <p>ISCA Submissions Co-chair</p> <p>Reviewer, Journal of Ambient Intelligence and Smart Environments</p> <p>President, Cornell India Association, Cornell University</p> <p>Reviewer, ACM TACO</p> <p>VP Logistics, Cornell India Association, Cornell University</p> <p>Member, ECE Graduate Organization, Cornell University</p>	<p>2017</p> <p>2017</p> <p>2015</p> <p>2015, 2017</p> <p>2013</p> <p>2013</p> <p>2012 – 2013</p> <p>Spring 2013</p>
PERSONAL DETAILS	<p><i>Citizenship:</i> India</p> <p><i>Visa Status:</i> F-1 (Student Visa)</p>	

REFERENCES

Prof. David H. Albonese
333 Rhodes Hall, Cornell University
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dha7@cs1.cornell.edu

Prof. Zhiru Zhang
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Dr. Srihari Cadambi
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Prof. Brandon M. Hency
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Wright-Patterson Air Force Base, OH
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bhency@gmail.com

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7171 Southwest Parkway
Austin, TX 78735
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